Amplifier development for multiplexed cryogenic detectors

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Abstract. We make some considerations on the question of driving the cable from the cryogenic stage of refrigerators to the room temperature, in the case of multiplexed detector array systems where a high total Shannon information capacity is required. We have constructed large SQUID arrays for the purpose, some of which exhibit lower than 5×10^{-8} Φ_0 $Hz^{-1/2}$ flux noise at 4.2 K and do not require magnetic shielding in a typical laboratory environment. The option of using class-D amplifiers to reduce the cryogenic heat load is briefly reviewed.[1]

1. Shannon capacity and multiplexing

The problem of reading out arrays cryogenic detector pixels, typically Transition Edge Sensors (TES), involves passing the combined Shannon information flow of the detectors from the cryogenic stage to room temperature electronics. The Shannon capacity [1] required for the signal path can be expressed as $C = \frac{1}{2}\Delta f \log_2\left(D^2/\Delta f\right)$ [bit/s] where Δf is the bandwidth and the power dynamic range D^2 is the ratio of the maximum signal power to the power spectral density of the noise floor. When considering a system where an amplifier (coldamp) at a low temperature T_0 drives a resistive cable leading to a higher temperature T_1, there are indications [2, App. B] that a given Shannon capacity might come at a cost of unavoidable heat production dQ/dt at T_0. Here dQ/dt is the sum of heat leakage through the cable and coldamp dissipation. If dQ/dt and C were linearly related it would make no difference in a N-pixel system whether N highly resistive but low-C cables, or one well conducting cable with capacity $N\times C_1$ were used. Here C_1 is the Shannon information flow generated by a single pixel. In practice, the single cable alternative tends to be mechanically easier to construct.

Before summing into a single cable, each of the N signals must be labeled to facilitate their separation later on. We adopt a model where this is performed by multiplying each signal by a different member of an orthogonal basis set [3]. The process is called multiplexing.

The resulting combined information flow requires a coldamp having at least the Shannon capacity $N\times C_1$. Because complicated circuitry would be required to trade Δf for D or vice versa, typically the Δf and D of the coldamp must be separately matched with the detector system properties. In this paper we consider the question of obtaining sufficient D, and leave Δf -related deliberations elsewhere.

2. Cable driving dc SQUIDs

The high dynamic range D implies that the SQUID output power, attenuated by the cable loss, must exceed by factor D^2 the noise floor of the room-temperature amplifier (LNA) and the Johnson noise in

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the cable. For large output power, large SQUID arrays and/or high-power constituent SQUIDs are needed.

2.1. A short note on bandwidth issues

The SQUID rather than the cable becomes often the Δf limiting element. The basic amplification mechanism of the SQUID extends in frequency space up to a fraction of the Josephson frequency. To enhance this, a higher operating point voltage is needed. This, together with the requirement to drive a typical cable termination impedance, again implies a high-power operation.

The dominant bandwidth limitation is typically the magnetic coupling through the input coil. We seek to improve this by utilizing distributed amplifier techniques [4] and Guanella transformers.

2.2. Role of linewidth in construction of large arrays

The primary challenges when constructing large SQUID arrays include (i) guaranteeing coherent operation of the constituent SQUIDs, and (ii) avoiding parasitic feedback mechanisms which jeopardize stability of the array. Use of narrow superconducting structures helps in avoiding flux traps which tend to spoil the coherence. The stability is often deteriorated by capacitive parasitic feedback [5], whose effectiveness scales proportional to the voltage gain $dV/d\Phi$ of the array and the total capacitance between the input coils and SQUID loops. The high $dV/d\Phi$ is the primary motivation to build arrays in the first place, but the total capacitance can be reduced by narrowing the lines.

To demonstrate, we show devices from three different lithography generations. Figure 1 shows a device fabricated by the standard VTT contact lithography with 3 μm linewidth and 2 μm gap between the lines. The SQUID loops are 20 μm wide, which facilitates the array operation without flux traps. The distorted characteristics indicate capacitive feedback, however.

A device fabricated using a tighter version of the contact lithography with 2 μm linewidth and 1.5 μm gap (Fig. 2) shows well-behaved flux response and very low flux noise when read out with a homemade dc-coupled SiGe amplifier [2]. In this experiment the amplifier was operated in non-terminated mode, and voltage-sampling positive feedback [6] - better known as APF [7] - was used to reach the $4.5 \times 10^{-8}\ \Phi_0\ \mathrm{Hz}^{-1/2}$ flux noise level. APF also increases R_D of the SQUID from its non-fedback value, which leads to a rather low cutoff frequency due to the capacitance of the dipstick wiring.

Recently, we have set up a SQUID fabrication process utilizing projection lithography and the Canon i-line stepper available in the VTT cleanroom [8]. Figure 3 shows characteristics and noise of a device obtained by bonding in series the two 60-SQUID arrays on a single chip. The SQUID loop geometry is the same as in Fig. 2 but a 3-turn (rather than 2-turn) input coil is fitted underneath the SQUID loops. Both this and previous device can be cooled in the earth magnetic field. Also the noise spectra in figures 2, 3 were recorded without superconducting or mu-metal shields.

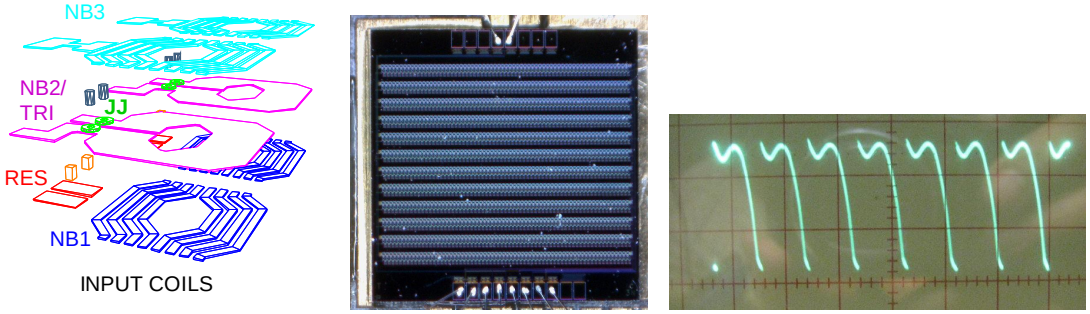

Figure 1. Left: structure of the constituent cells of the 66-series 12-parallel SQUID array, utilizing 3 μm / 2 μm design rules. Middle: microphotograph of the SQUID array chip. Right: flux-to-voltage characteristics are distorted owing to parasitic capacitive feedback, which also degrades the flux noise level.

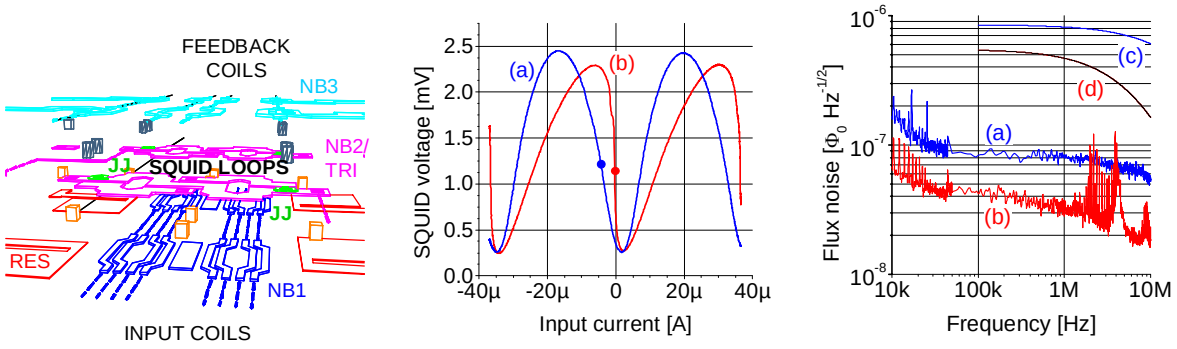

Figure 2. Left: structure of the constituent cells of the 80-series 6-parallel SQUID array, exploiting 2 µm / 1.5 µm design rules. Middle: flux-to-voltage characteristics (a) without and (b) with APF, noise measurement setpoints indicated. Right, the SiGe LNA output noise, scaled into flux noise by the system gain measured at 100 kHz, (a) without and (b) with APF. The frequency response relative to its 100 kHz value is indicated (c) without and (d) with APF.

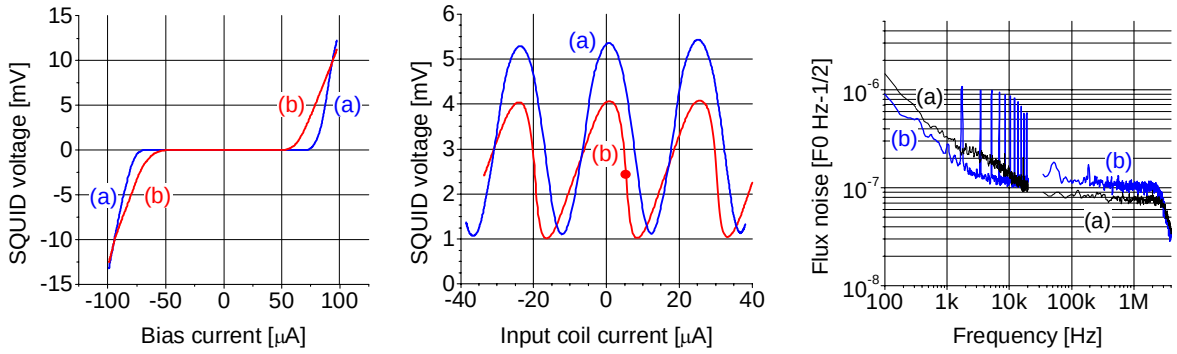

Figure 3. Left: current-to-voltage characteristics of the 120-series array at (a) $n\Phi_0$ and (b) $(n+½)\Phi_0$ applied flux, with 1 µm linewidth and 1 µm gap in input coils. Middle: flux-to-voltage characteristics (a) without and (b) with APF. Right: flux noise measured on the steep slope of the flux characteristics, using (a) the SiGe LNA and (b) the INA163 instrumentation amplifier.

2.3. Power efficiency of dc SQUIDs

The static power dissipation of the dc SQUID can be calculated from their analytically solvable overdamped characteristics as $P_D = 0.63 R_S I_C^2$ in terms of the shunt resistance R_S and the junction critical current I_C. This corresponds to the setpoint where the load line slope equals the dynamic resistance R_D = 1.0 R_S of the $\Phi_A = \Phi_0 / 4$ SQUID characteristic at their intersection. At this setpoint the full ±0.25 Φ_0 flux swing corresponds to the $P_O = 0.027 R_S I_C^2$ available output power. In practice the tolerated flux swing is restricted to a lower value by the distortion tolerated by the application. Local negative feedback [6] can exploited (Fig. 4) to expand the swing and hence to improve the dynamic range *D*. For the noise optimal β_C = 0.7 β_L = 1 SQUID a numerical procedure yields $P_D = 0.54 R_S I_C^2$, $P_O = 0.011 R_S I_C^2$ and R_D = 1.3 R_S. Hence the efficiency of the dc SQUID as an amplifier is less than 5%. Choice of a non-matched load line may improve efficiency, but leads to bandwidth difficulties because the cold end of the cable will not be properly terminated.

3. Class-D amplifiers

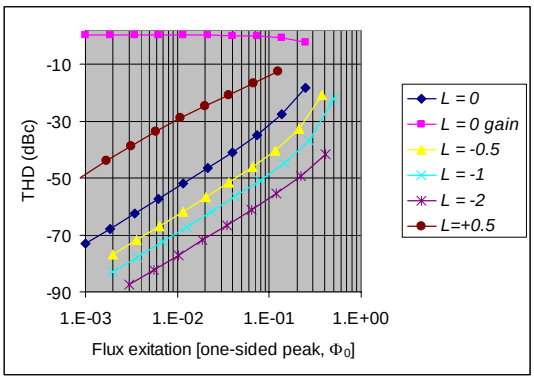

Figure 4. Numerically calculated total harmonic distortion due to a $\beta_C = 0.7$ $\beta_L = 1$ dc SQUID, with local feedback at various loop gains L.

The drive power level of several μW required from the coldamp approaches the regime served well by semiconductor amplifiers, such as SiGe BJTs [9]. When operated as class-A the power efficiency is not significantly better than SQUID arrays, however. An obvious way to enhance the coldamp efficiency is to utilize the class-D operation, where the active device acts as a switch. We have experimented with the concept by using a CMOS ramp generator and as the comparator either the BU7251 which functions in LHe with supply voltage V_{DD} > 3.7V or the OPA2320 with V_{DD} = 2.3 … 2.6 V (Fig. 5). The reached power dissipation has not been satisfactory so far, unfortunately.

Ultimately a Josephson junction based amplifier appears more advantageous, such as a push-pull configuration of two dc SQUID devices, dimensioned for poor matching to the load both in the voltage state ($R_D >> R_{load}$) and in the superconducting state (0 Ω << R_{load}). Note that the dynamics of an ordinary dc SQUID already resembles class-D amplifiers in the sense that the signal is constructed as pulse width modulation of the Josephson oscillation [10]. An attempt to reduce the dissipation during the switching event i.e. quantum phase rotation has led to concepts of the hg SQUID and the un SQUID [11, 12].

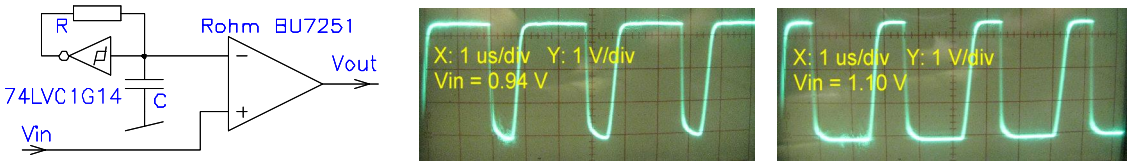

Figure 5: A simple class-D CMOS amplifier demonstration at T = 4.2 K. R = 100 kΩ, C = 0 pF.

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