A post-SQUID ac amplifier aimed for multiplexed detector readouts

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***Abstract*— We have built a room-temperature amplifier based on Si JFETs intended for ac-coupled SQUID readouts, such as frequency-domain multiplexed transition-edge sensor systems. The amplifier operates at 5 MHz center frequency where it has the measured noise temperature of 27 K for a 60-ohm load, which includes the noise from the active termination and the room-temperature transformer. When driven from a SQUID with an on-chip matching transformer flux noise of 0.45 $\mu\,\Phi_0\ \mathrm{Hz}^{-1/2}$ has been obtained. Additionally, we consider the potential of the recently introduced SiGe bipolar transistors for the same application. The dynamic range considerations in SQUID multiplexers, which require the use of an amplifier with a low noise temperature, are briefly discussed.**

I. Introduction

THE achieved noise level in dc SQUID systems is often dominated by the first room-temperature amplifier stage. A simple calculation based on autonomous-SQUID equations reveals that the noise temperature at the output of a dc SQUID having no excess noise is theoretically 2.4 times the cryogenic bath temperature T_{cr} , assuming $\beta_c = \beta_L = 1$ but regardless of other design parameters. Such noise temperature is difficult to reach by semiconductor devices even when T_{cr} = 4.2 K and even more difficult if the SQUID is operated at sub-kelvin temperatures. Reduction of the system noise is particularly important when one needs a large dynamic range, limited by the noise floor at the low end and by the maximum tolerated non-linearity at the high end. Such a need is particularly pressing in frequency-domain multiplexed (FDM) readouts of cryogenic detectors [1], but similar need appears also in time-domain multiplexing (TDM) [2].

II. Need for Dynamic Range

A. Dynamic range budget

A serious design constraint in SQUID multiplexers is the dynamic range requirement in the signal path, simultaneously with a sufficient bandwidth [3]. The dynamic range ceiling is usually determined by the SQUID nonlinearity. The dynamic range floor is determined by the SQUID flux noise, whose value can be multiplied by $\sqrt{2}$ to take into account the contribution of the back-action noise in the case where SQUIDs are noise matched to the cryogenic sensors.

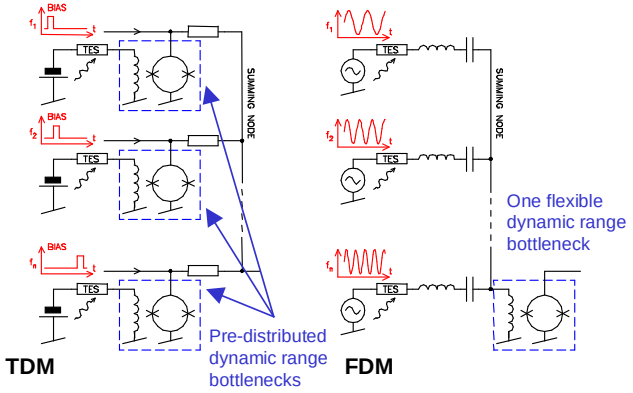

Figure 1: The distribution of the dynamic range budget in time domain and frequency domain multiplexers.

The flux noise Φ_n of dc SQUIDs (including SQUID arrays) is related to the SQUID power dissipation P_d by

$$P_d > 6.8 k_B T \left(\frac{\Phi_0}{\Phi_n} \right)^2 . \qquad (1)$$

For example, a SQUID with $\Phi_n = 10^{-7}\Phi_0 /\sqrt{\mathrm{Hz}}$ dissipates at least 0.94 nW at 100 mK. Because of the typical limit in the available cooling power, there is also a limit on the total dynamic range budget of the readout system. This dynamic range budged can be distributed in different ways: eg. there can be a single SQUID with a large power dissipation and small Φ_n (and consequently a large dynamic range), or a number of SQUIDs with smaller dissipation and a smaller dynamic range.

Note that there is a difference between TDM and FDM in the way the dynamic range budget is distributed between the pixels [3] (Fig. 1). In the preferred TDM circuit topology the distribution is hard-wired so that each pixel always gets an equal fraction of the total dynamic range budget. This does not matter in bolometer systems, where there is a signal present in all the pixels at all the time. Contrary to this, in the preferred FDM circuit topology the signals from a number of pixels are summed before feeding them into a single SQUID bottleneck. If non-zero signal is expected simultaneously from a few pixels only, as is the case in photon-counting

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calorimeters, the active pixel(s) can temporarily use the total dynamic range budget, including that of the neighboring idle pixels. Thus FDM has an advantage over TDM in calorimeter readouts.

B. *SQUID non-linearity*

A voltage-biased SQUID has more linear flux response than the same SQUID in current-biased configuration (Fig. 2). In order to get a crude estimate on the size of the effect, we have simulated numerically Josephson dynamics of an autonomous dc SQUID with β_C = 0.6 and β_L = 1, and made a polynomial least-squares fit to the flux response at 0.2 Φ_0 above the curve minimum. The simulations were performed at bias points close to the maximum modulation depth. These choices reflect a typical (but linearity-wise, probably non-optimal) choice of the operating point in a real SQUID system. For the voltage bias the obtained fit is $I_{SQ} = I_0 + \partial I/\partial\phi\left(\phi - 0.48\phi^2 + 0.45\phi^3 + 2.5\phi^4 - 46\phi^5\right)$ whereas for the current bias it is $U_{SQ} = U_0 + \partial U/\partial\phi\left(\phi - 3.3\phi^2 - 9.1\phi^3 - 11\phi^4 - 22\phi^5\right)$, where ϕ is the deviation from the setpoint in the units of flux quanta. A similar fit to the characteristics of a real dc SQUID [4] with a voltage-like bias from a 0.5 Ω source yields $I_{SQ} = I_0 + \partial I/\partial\phi\left(\phi - 0.65\phi^2 - 2.2\phi^3 + 5.5\phi^4 - 14\phi^5\right)$.

The SQUID linearity is a crucial bottleneck in design of an FDM system [5]. When measuring the energy of a registered photon, i.e. area of the current pulse from the TES with an accuracy of 10^{-4} , the quadratic non-linearity limits the tolerable flux excursion below 4×10^{-4} Φ_0 in the voltage-biased case and below 6×10^{-5} Φ_0 in the current-biased case. Negative feedback, fortunately, linearizes the response not only by reducing the flux excursion and thus reducing the generation of the nonlinear signal, but by additionally feeding back the (partial) correction for the remaining nonlinear signal[1]. This means that a reasonable closed-loop gain, possibly in conjunction with post-distortion of the signal, leads to sufficient linearization.

The post-SQUID amplifier stage is important because it must not degrade the SQUID noise, as this would decrease the available dynamic range and increase the need for the hard-to-obtain loop gain further.

C. *Two-stage SQUID amplifier*

Design of a room-temperature amplifier capable to undercut the output noise temperature of a SQUID at 4.2 K is a challenging task. The challenge can be alleviated by using a second cryogenic amplifier stage, which, however, must not become the dominant dynamic range bottleneck. One possibility is to use a *n*-SQUID series array [6], which is capable to deliver more signal power to the room-temperature amplifier than a single SQUID. The important design parameter is then the flux ratio $k_f = (\partial I/\partial\phi)_1 \times M_2$ which tells how many flux quanta are induced in each constituent SQUID of the array when one flux quantum is applied to the first SQUID. k_f depends on the current gain $\partial I/\partial\Phi$ of the 1st SQUID

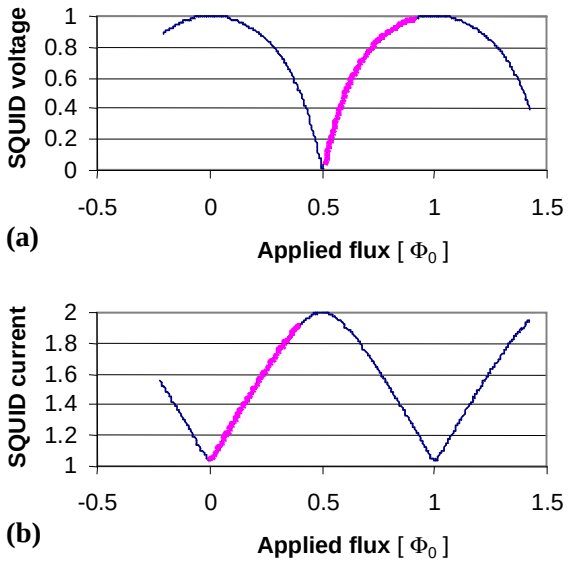

Figure 2 : Simulated flux response of (a) current biased and (b) voltage biased dc SQUID. The visible ripple is the Josephson oscillation remaining after signal averaging. Least squares fits to a 5th order polynomial are depicted.

and mutual inductances M_2 of the SQUIDs forming the array. If one chose[2] $k_f \approx 0.15$, the second-order nonlinearities of the (typically) voltage-biased 1st SQUID and the current-biased array SQUID would contribute equally to the total non-linearity. Writing the noise temperature T_n at the output of a single SQUID (n = 1) or a SQUID array (n > 1) as

$$4k_B T_n = \left(\sqrt{n}\Phi_{n2}\frac{\partial V}{\partial\Phi}\right)^2 / (nR_d) \qquad (2)$$

in terms of flux noise Φ_{n2} and voltage gain $\partial V/\partial\Phi$ of each constituent SQUID suggests that the T_n does not change when n is increased. If flux noise Φ_{n1} of the 1st SQUID rather than the self-noise of the array dominates, one can write

$$4k_B T_n = \left(n k_f \Phi_{n1}\frac{\partial V}{\partial\Phi}\right)^2 / (nR_d) \qquad (3)$$

and higher noise temperatures than ~2.4×T_{bath} at the output become possible. Note, however, that one would need in the order of $n > 1/k_f^2$ SQUIDs in series before the noise floor will be dominated by the 1st SQUID, which may be quite large a number[3]. Even larger n is required in practice because the power dissipation typically forces one to put the array at T_2 = 4.2 K rather than T_1 = 100 mK stage, which means $\Phi_{n2} > \Phi_{n1}$. The above constraint is replaced by $n > T_2/(T_1 k_f^2)$ in this case. One would conclude that a low-T_n post-SQUID amplifier is necessary even in the case of the two-stage SQUID amplifier in order to avoid ridiculously large SQUID arrays.

[1] In the FDM, however, the *n*:th order correction is at *n* times the carrier frequency, affecting the closed-loop bandwidth requirement.

[2] Ratio of the 2nd order nonlinearity coefficients in voltage- and current-biased cases.

[3] Identical SQUIDs assumed for the 1st SQUID and for the constituent SQUIDs of the array.

III. Room-temperature semiconductor devices

Bipolar transistors such as MAT03 [7], SSM2220 [8] or bipolar-input operational amplifiers AD797, LMH6624 has been used often as the amplifying elements in post-SQUID amplifiers. Their voltage noise is usually modelled [9] to be due to the base spreading resistance R_{BB} and the shot noise due to collector current I_C reacting on the base-emitter junction

FET type [publication]	T_n @ 5MHz	R_{opt}@ 5MHz
Toshiba 2SK146/7 [12]	19 K	690 Ω
Interfet IF1320 [13]	13 K	2.6 kΩ
Interfet IF3602 [14]	4 K	170 Ω
Philips BF862	2.1 K	5.2 kΩ

Table 1: Theoretical noise temperatures of some JFETs.used in post-SQUID amplifiers.

$$(u_n)^2 = 4k_B T R_{BB} + \frac{2(k_B T)^2}{eI_C}. \quad (4)$$

and the current noise is the shot noise due to the base current

$$i_n = \sqrt{2eI_C / h_{fe}}. \quad (5)$$

When neglecting R_{BB} and combining the expressions into

$$T_n = T / \sqrt{h_{fe}}, \quad (6)$$

one notices that extremely large values of current gain h_{fe} are needed to reach T_n below ~ 20 K. Usually the R_{BB}-related term dominates so that the T_n reachable in practice is even worse. This applies to eg. Zetex FZT690 for which we have measured u_n ~1 nV Hz$^{-1/2}$ implying T_n = 36 K regardless of its high h_{fe} = 1400.

The advantages of bipolar transistors are (i) T_n does not depend on frequency, and (ii) noise matching resistance $R_{opt} \approx \sqrt{h_{fe}} \times 26\,\mathrm{mV} / I_C$ tends to be reasonably close to the source resistance of the SQUID.

For JFETs the noise equations from [9] at frequency f can be combined into

$$T_n = T \; f / f_n \quad (7)$$

where the 'noise bandwidth'

$$f_n = g_m / 2\pi C_g \quad (8)$$

depends on the FET fabrication technology. The above noise temperature is reached for a resistive source only when the noise matching condition

$$R_{opt} = 0.26 / f C_g \quad (9)$$

is met. In commercialy available discrete silicon JFETs the f_n can approach 1 GHz, whereas for GaAs and InP MESFETs and HEMTs f_n may be tens or hundreds of GHz. GaAs- and InP-based devices have in the past been considered useless in the low-MHz frequency range because of their high 1/f noise, but there are some sub-nanovolt noise levels obtained recently [10][11] at cryogenic temperatures.

The characteristic values for a few JFET types calculated at 5 MHz which have been used in readouts of cryogenic circuits are depicted in Table 1. Among those, the BF862 is the most promising type, because of its large ratio of transconductance g_m to input capacitance C_g.

The R_{opt} values tend to be too high for SQUID readout. Impedance transformation is then necessary, by (i) coupling several FETs in parallel, (ii) using a transformer, or (iii) coupling several SQUIDs in series.

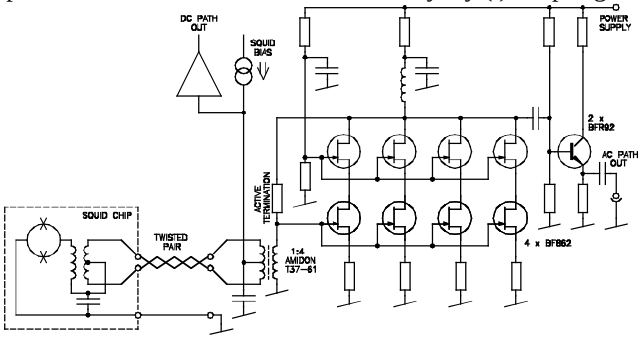

Figure 3: Simplified schematic of the amplifier

IV. Amplifier design

We have constructed an amplifier card (Figs. 3 and 4), also containing the circuits needed for SQUID bias and test signal feeds [15]. The first stage of our amplifier consists of four FET cascodes coupled in parallel. The input noise resistance level is further decreased by a 1:4 transformer, wound on an Amidon T37-61 toroidial core. Stray inductance of the transformer has been used to tune out the gate-source capacitance of the FETs in the operating frequency range. The cascode circuit reduces the bandwidth-limiting effect due to the gate-drain (Miller) capacitance of the lower FET. The gate-drain capacitance of the upper FET has been tuned out by an inductor in the drain. Each JFET is operated at 10 mA drain current.

Active negative feedback has been utilized to realize an effective 960 Ω resistive load at the cascode input, which over the transformer acts as a 60 Ω termination suitable for twisted pairs. The –3 dB band of the amplifier extends from 1.8 MHz to 7.8 MHz. The nominal voltage gain is 700 V/V. A simplified schematic is shown in Fig. 3. There is a separate dc-coupled signal path containing the SQUID bias circuitry and an AD797 -based low frequency amplifier for monitoring the SQUID setpoint.

V. Measured noise

The noise performance of the amplifier was measured at 5 MHz using 10 Ω, 50 Ω, 100 Ω, 200 Ω and 560 Ω resistors as input terminations at 294 K and 77 K. The noise temperatures were then calculated using the Y-factor method. The 50 Ω figure was further checked with the source resistor at 4.2 K. The results are shown in fig. 5. The data fits well to a model having the input-referred voltage noise of u_n = 0.21 nV Hz$^{-1/2}$ and current noise of i_n = 3.5 pA Hz$^{-1/2}$. This would

translate into the optimal noise temperature of T_n = 27 K and noise matching resistance of R_{opt} = 60 Ω.

The reached noise temperature is above the theoretical value, for reasons which require further investigation. In order

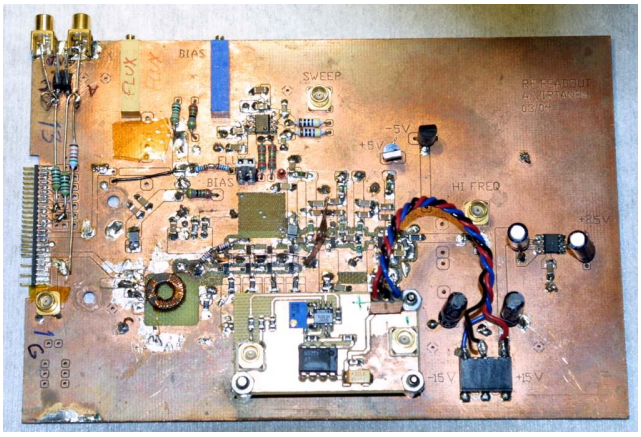

Figure 4: Photograph of the amplifier prototype card.

to rule out the contribution of the transformer core losses, the transformer was tuned with a capacitor and a Q-factor of 126 was measured. This translates into a ~2 K contribution to T_n. The modeled noise contribution from the feedback resistor does not explain the discrepancy, either. Some remaining candidates for the cause are (i) more complex system-level interaction between the amplifier stages, (ii) noise or rectified rf interference coupled from supply/bias lines, or (iii) the FETs not reaching their theoretically-estimated performance, even approximately.

A comparison with pre-existing designs such as [7] (T_n = 77 K) , [8] (T_n = 89 K), [13] (T_n = 45 K, scaled from 16 MHz into 5 MHz), or the AD797 op-amp (T_n = 65 K) is a bit unfair because the above designs are optimized for a different application and with different constraints, but it puts the the noise temperature achieved in this work to some sort of a perspective.

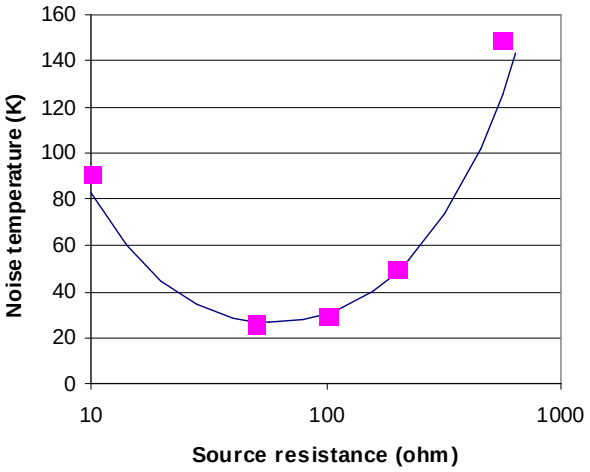

Figure 5: The measured noise temperature of the amplifier at f = 5 MHz with various source resistances. A fit to the model u_n = 0.21 nV/√Hz and i_n = 3.5 pA/√Hz is depicted.

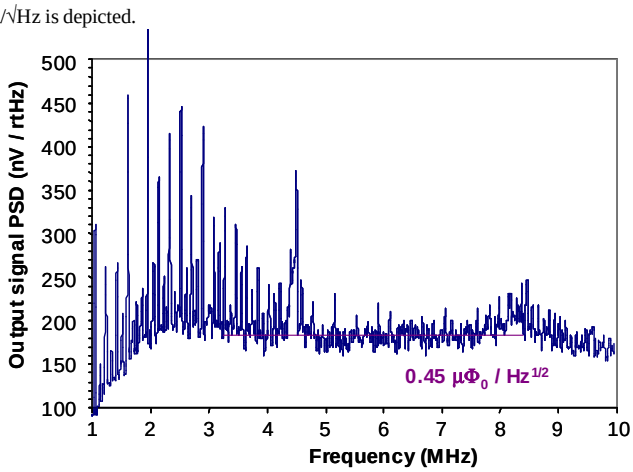

Figure 6: Noise spectrum at the amplifier output when operated with a SQUID. The measured transfer function is 380 mV / Φ_0 at 6 MHz.

The amplifier was also coupled to a washer-type SQUID [4] having an on-chip integrated 1:5 output transformer. The transformer boosts the SQUID dynamic resistance $R_d \approx 1.2$ Ω into 30 Ω level and the SQUID gain $\partial V/\partial \Phi \approx 200$ μV/Φ_0 into 1 mV/Φ_0 level at frequencies above ~2.5 MHz. A flux noise level of 0.45 $\mu\Phi_0/\sqrt{\text{Hz}}$ at 5 MHz was measured with the JFET electronics when the SQUID was operated at 4.2 K. This is slightly more than the 0.36 $\mu\Phi_0/\sqrt{\text{Hz}}$ one would compute from the SQUID parameters and the amplifier noise data above. The measured noise spectrum in fig. 4 suffers from interference originating from the spectrum analyzer, which may explain the excess noise.

VI. SiGe Bipolar Transistors

We have experimented with a number of SiGe bipolar transistors. Most notably, the Infineon BFP650 has exhibited voltage noise below 0.3 nV $\text{Hz}^{-1/2}$ at room temperature and below 0.2 nV $\text{Hz}^{-1/2}$ at 4.2 K (Fig. 7). The room-temperature white voltage noise is consistent with Johnson noise from R_{BB} = 1.5 Ω and I_c = 5 mA shot noise acting on the B-E junction (Eq. 4). At room temperature the SiGe-based amplifier has the advantage of lower power consumption than one utilizing the BF862 JFETs. At cryogenic temperatures the reduction of the noise temperature is not very large, but it is more important that 4.2 K operation (i) opens the possibility to use short negative feedback for increasing the SQUID dynamic range, and (ii) avoids the noise contribution due to Johnson noise in the cryostat wiring. There are indications [16] that the power consumption of the SiGe devices could be reduced into sub-mW range, which would facilitate multi-channel operation in closed-cycle refrigerators.

VII. Conclusion

The high-frequency noise performance of our amplifier compares favourably with pre-existing designs and is

comparable to the recently introduced wideband electronics [17]. Its performance is likely to be exceeded, however, by applying SiGe discrete bipolar transistors which have become

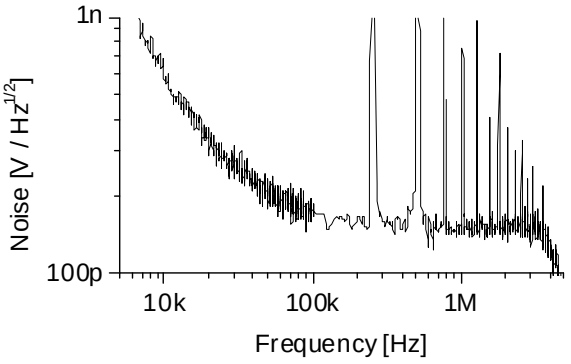

Figure 7: Noise spectrum of the BFP650 transistor at 4.2 K with a 3.3 Ω resistor as the input termination. The bias point is Ic = 5 mA and Vce = 1.5 V. The 4 MHz cutoff is due to the cable capacitance of the dipstick.

available recently. The JFET amplifier described in this paper remains still an useful building block for experimenting with frequency-domain multiplexed sensor arrays.

VIII. Acknowledgement

We thank Jan van der Kuur and Piet de Korte for contributions to the TDM vs FDM comparison and on the effect of nonlinearities, which are worth a dedicated separate paper.

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