Jena E-SQUID process v1.1 , inserted here for compatibility checking only				
GDS	**Name**	**Patterned layer**	**d (nm)**	**Remarks**
-		SiO2 (thermal)	400	
01	M0	Nb	200	
02	I0A	Nb2O5 (anodized)	50	M0 surface anodized to 25V
02	I0A	SiO2 (CVD)	100	Lift-off with anodization mask
03	I0B	SiO2 (CVD)	100	
05	M1	Nb	250	
06	T1	Nb/Al-AlOx/Nb	60/12/30	On top of M1
07	I1A	Nb2O5 (anodized)	70	M1-T1 surface anodized to 35V
08	CUT			Cut conductors to anodization
09	I1B	SiO2 (CVD)	200	
10	R1	AuPd	100	Resistors, lift-off
11	I2	SiO2	100	
12	M2	Nb	350	
13	R2			Optional bondable metal on pads

VTT E-SQUID process 2012-v2 , SPCR-based				
GDS	**Mask name**	**Deposited/Patterned layer**	**d (nm)**	**Remarks**
-		SiO2 (thermal)	200	Blanco layer
50	MARK			Chip numbers, full-wafer mask. Also GND contacts
51	NB1	Nb	200	
52	INS1	SiO2 (PECVD)	250	
53	CER	Nb/Al-AlOx/Nb	250/10/ 70	CER mask removes Al-AlOx(10nm) + Nb(70nm) counterelectrode, leaves Nb(250nm) base electrode
54	ANOD	-“”-	50	Anodize junction sidewalls to 22V
55	NB2	-“”-		Pattern the Nb(250nm) base electrode GDS layer number chosen for Jena-compatibility
-		SiO2 (PECVD)	270	Blanco layer, unpatterned so far
56	RES	TiW	150	Resistors, 4W/ •
57	INS3	SiO2 (PECVD)	100	Vias NB3->RES
58	INS2	Patterns the previous SiO2’s (100 + 270nm)		Vias NB3->NB2 GDS layer number chosen for Jena-compatibility
59	NB3	Nb	350	
60	PASS			Optional passivation, holes over pads Optional bondable metal on pads

VTT E-SQUID design rules

- The process based on SPCR step coverage control rather than CMP
- The chosen insulators thicknesses should leave 250 nm NB1-NB2 separation, 370 nm NB2-NB3 separation and 520 nm NB1-NB3 separation. This is first step in attempting same sheet inductances as in the Jena process. Another effect is the London penetration depth, which is so far unknown for this process, we assume $l_L \approx$ 90 nm.
- Sheet capacitances between the Nb metal layers will be slightly different from Jena values, due to Jena insulation stacks containing both Nb_2O_5 and SiO_2, whereas VTT stacks are pure SiO_2.
- The goal critical current density is J_C = 100 A/cm^2.

1. Layer NB1

1.1. Line width w ³ 2.0 mm. Expected[1] to shrink Dw ≈ 0.2 mm relative to mask.
1.2. Line-to-line separation ³ 1.5 mm.

2. Layer INS1

2.1. Smallest via 3.0 x 3.0 mm.
2.2. NB1 must fully cover the via and NB1 edges must reside ³ 1.5 mm outside the via edges.
2.3. NB2 must fully cover the via and NB2 edges must reside ³ 1.5 mm outside the via edges.

3. Layer CER

3.1. This determines the Josephson junction size. The JJ diameter d ³ 3.2 mm on mask. Expected[1] to shrink Dd ≈ 0.3 mm relative to mask, of which 0.1 mm is due to sidewall anodization. The smallest JJ is expected to have the realized diameter d = 2.9 mm.

4. Layer ANOD

4.1. Inner boundary of the anodized region is the CE edge, the outer boundary is the ANOD edge. CE-to-ANOD edge-to-edge distance ³ 1.5 mm. For example, for the smallest allowed Josephson junction the ANOD ring diameter will be 6.2 mm.
4.2. ANOD regions must reside inside NB2 regions, with ³ 0.2 mm edge-to-edge separation. The ³ 1.0 mm edge-to-edge separation is recommended whenever possible.

5. Layer NB2

5.1. Line width w ³ 2.0 mm. Expected[1] to shrink Dw ≈ 0.2 mm relative to mask.
5.2. Line-to-line separation ³ 1.5 mm.

6. Layer INS2

6.1. Smallest via 3.0 x 3.0 mm.
6.2. NB2 must fully cover the via and NB2 edges must be ³ 1.5 mm outside the via edges.
6.3. An exception to the size rule is the via leading to the top of a JJ. Here (a) the INS2 via must reside inside CE, (b) INS2-to-CE edge-to-edge separation ³ 0.8 mm, and (c) INS2 diameter (or smallest linear dimension) ³ 1.6 mm.
6.4. All cases: NB3 must fully cover the INS2 via; and NB3 edges must be ³ 1.5 mm outside the via edges.
6.5. In case of a stacked INS1+INS2 via, the INS1 via must be completely enclosed by the INS2 via. The INS1-to-INS2 edge-to-edge separation ³ 0.5 mm. The stacked via must have the NB2 metal present, with the standard overlap rules.
6.6. INS2 vias must reside outside RES regions, with INS2-to-RES edge-to-edge distance ³ 3.0 mm.
6.7. INS2 via is not allowed to lie over an NB1 edge. INS2-to-NB1 edge-to-edge distance ³ 3.0 mm.

7. Layer RES

7.1. Line width w ³ 6.0 mm. Expected[1] to shrink Dw ≈ 0.2 mm relative to mask.
7.2. Line-to-line separation ³ 4.0 mm.
7.3. RES must not cross any edge of a lower layer.

8. Layer INS3

8.1. Smallest via 3.0 x 3.0 mm.
8.2. RES must fully cover the via and RES edges must reside ³ 1.5 mm outside the via edges.
8.3. NB3 must fully cover the via and NB3 edges must reside ³ 1.5 mm outside the via edges.

9. Layer NB3

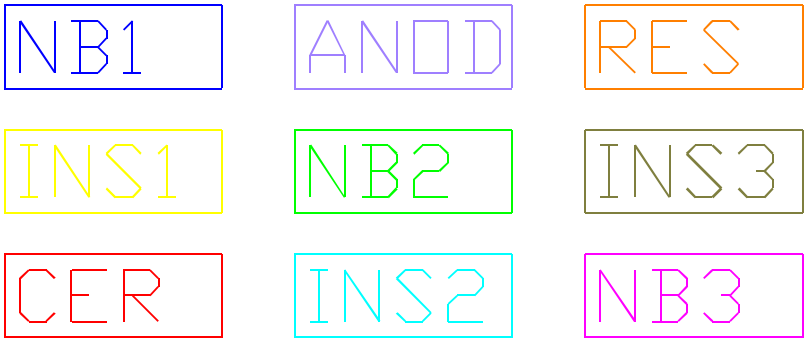
9.1. Line width w ³ 3.0 mm.
9.2. Line-to-line separation ³ 2.0 mm.

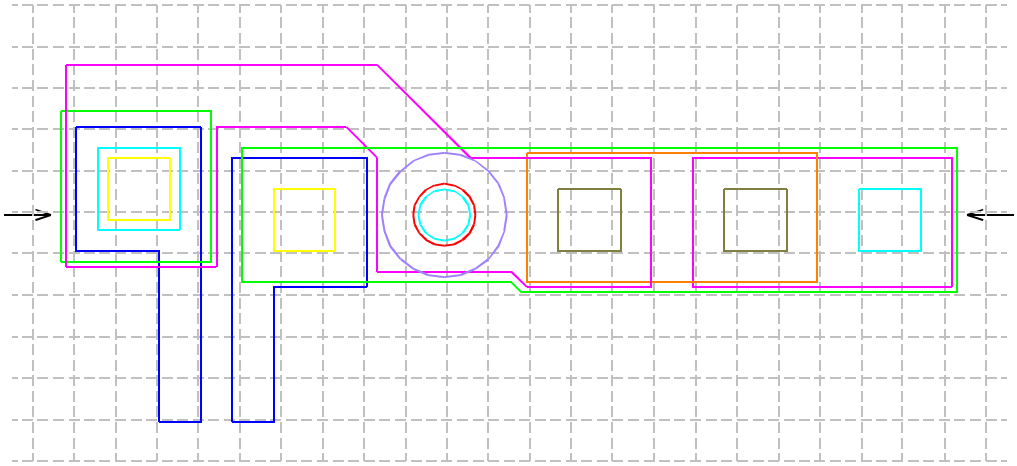
10. Miscellaneous

[1] Value not chcked yet or guaranteed, but given as an educated guess for the benefit of the designers.

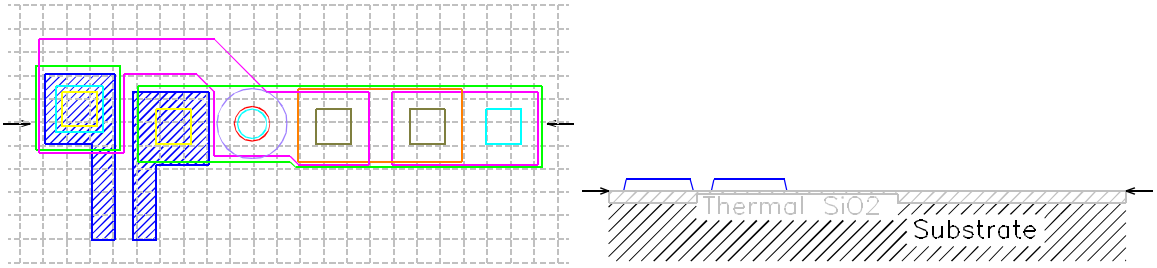
10.1. In order to avoid stacking many low steps into one high step, edges in any layers should not co-incide on top of each other. Rather, edge-to-edge separation ³ 0.2 mm should be retained.

An example layout

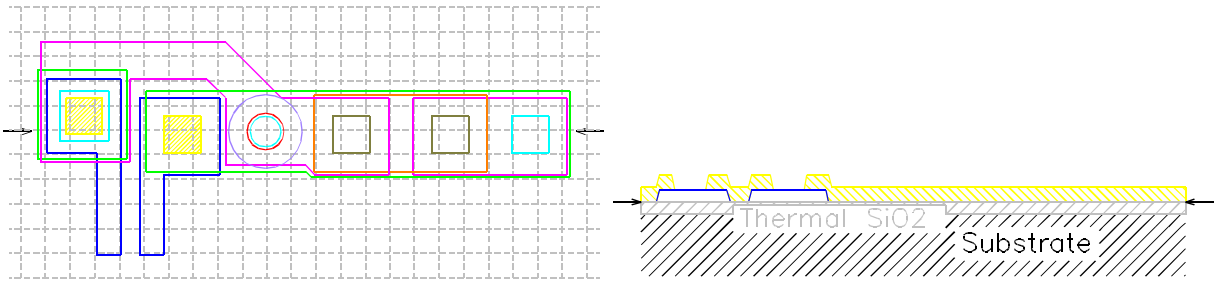




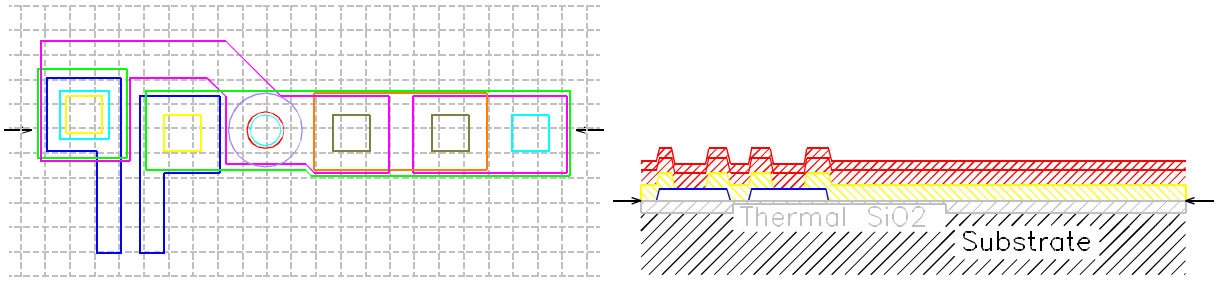
An example layout consists of a ø 3.2 mm Josephson junction (over)damped with a 5 W shunt resistor. Also shown is a 2 mm x 2 mm grid. The cross-section will be taken between the arrows.



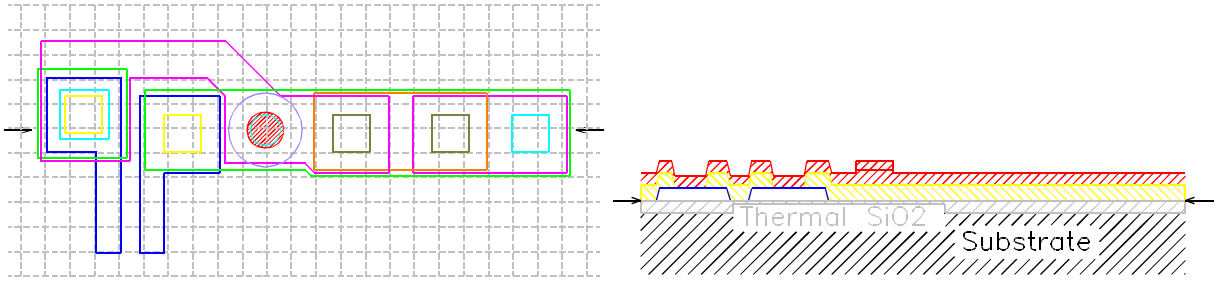
After deposition of the first Nb metal and patterning by the NB1 mask.



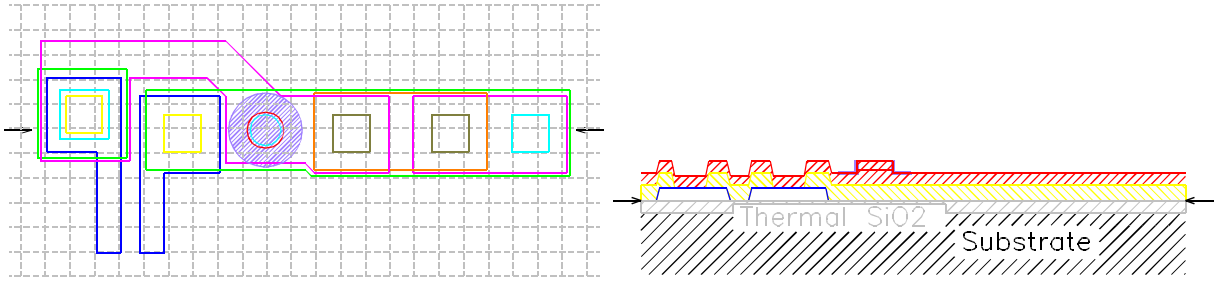
After deposition of the first SiO2 insulator and patterning by the INS1 mask.



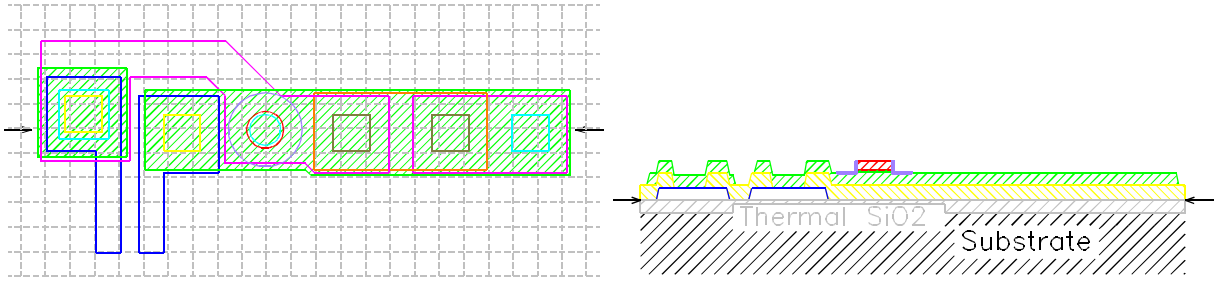
After deposition of the Nb/Al-AlOx/Nb trilayer.



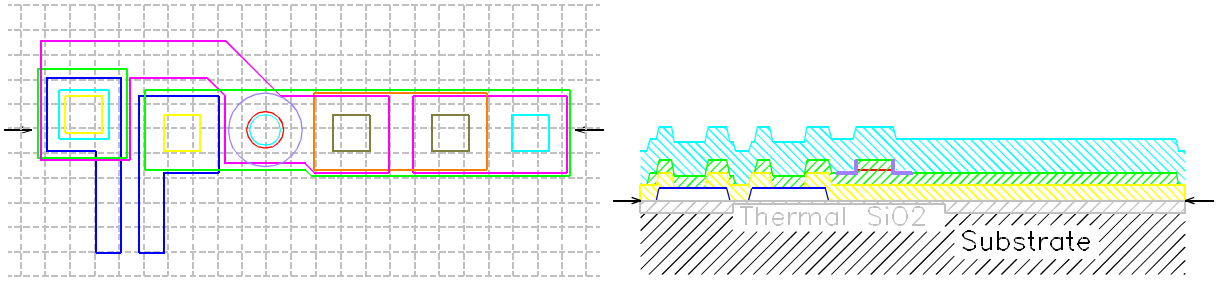
After patterning the counterelectrode by the CER mask.



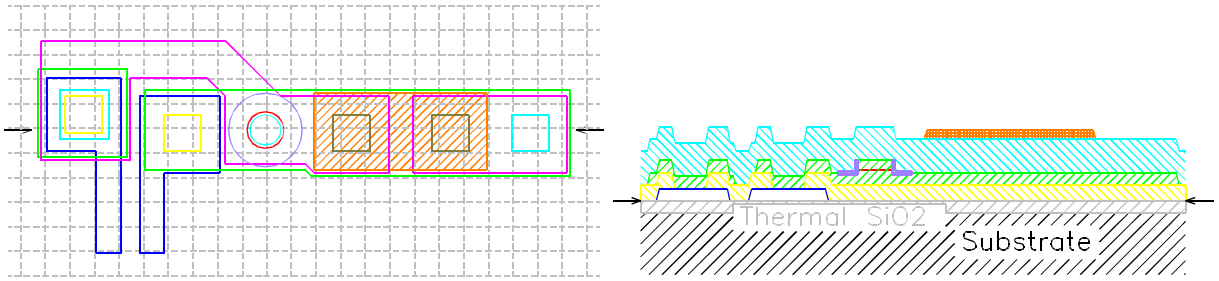
After anodization by the ANOD mask.



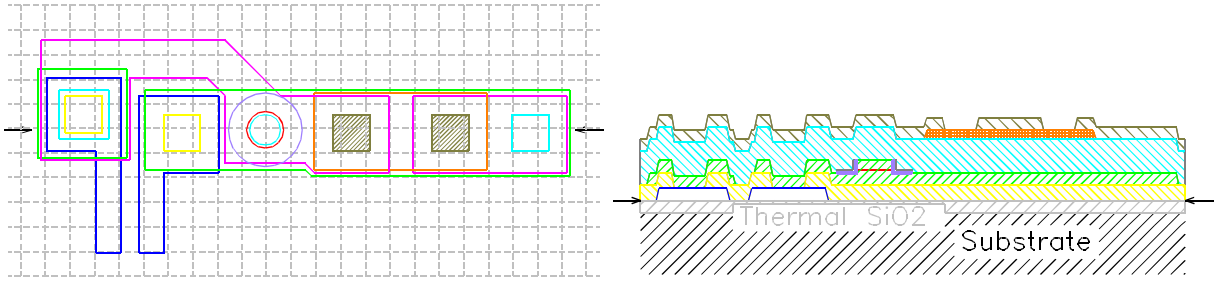
After patterning the base electrode by the NB2 mask. The base electrode color is changed to emphasize how it can be considered as the second Nb wiring layer.



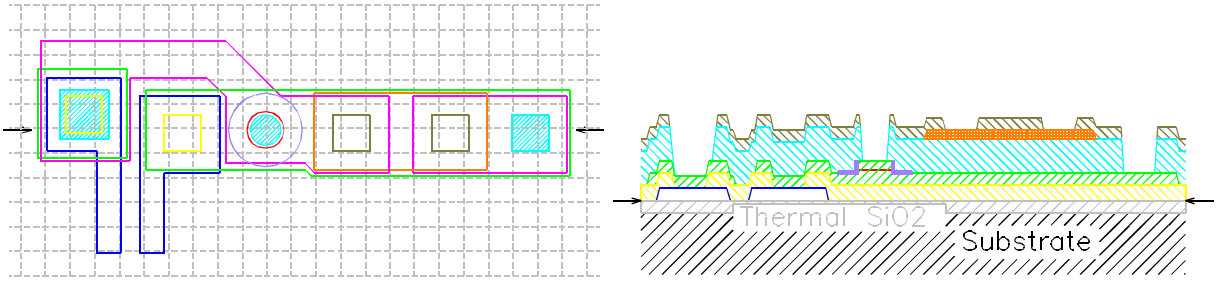
After deposition of second SiO2 insulator



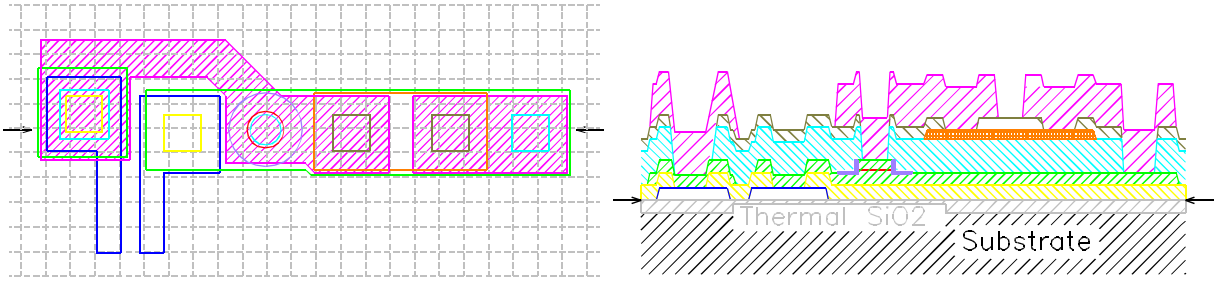
After deposition of the TiW resistor layer and patterning by the RES mask.



After deposition of the third SiO2 insulation and patterning by the INS3 mask.



After patterning by the INS2 mask.



After deposition of the third Nb metal and patterning with the NB3 mask.